09-28-04

EXPRESS MAIL NO. EV529823452US

AF CFW

OIPE SEP 27 2004 JC#0 PATENT & TRADEMARK OFFICE

TRANSMITTAL FORM

(To be used for all correspondence after initial filing)

Application Number	10/032,289
Filing Date	December 21, 2001
First Named Inventor	Sergio Tommaso Spampinato
Art Unit	2814
Examiner Name	Dana Farahani
Attorney Docket No.	853063.497

ENCLOSURES (*check all that apply*)

- [X] Fee Transmittal Form
  - [X] Fee Attached
- [ ] Amendment/Response
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement; Form PTO-1449
- [ ] Cited References
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts under 37 C.F.R. 1.52 or 1.53
- [ ] Response to Missing Parts/Incomplete Application
- [ ] Drawing(s)
- [ ] Request for Corrected Filing Receipt
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation, Change of Correspondence Address
- [ ] Declaration
- [ ] Statement under 37 CFR 3.73(b)
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD(s), Number of CD(s) _____
- [ ] After Allowance Communication to Technology Center (TC)
- [ ] Appeal Communication to Board of Appeals and Interferences
- [X] Appeal Communication to TC *(Appeal Notice, Brief, Reply Brief)*
- [ ] Proprietary Information
- [ ] Status Letter
- [X] Return Receipt Postcard
- [ ] Additional Enclosure(s) *(please identify below)*:

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Individual Name	Robert Iannucci – Reg. No. 33,514	Customer Number 00500
Signature		
Date	September 27, 2004	

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below.

Typed or printed name	Sent Via Express Mail	
Signature		Date:

EXPRESS MAIL NO. EV529823452US

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Sergio Tommaso Spampinato
Application No.	:	10/032,289
Filed	:	December 21, 2001
For	:	INTEGRATED DEVICE IN EMITTER-SWITCHING CONFIGURATION AND RELATED MANUFACTURING PROCESS

Examiner	:	Dana Farahani
Art Unit	:	2814
Docket No.	:	853063.497
Date	:	September 27, 2004

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPELLANT'S BRIEF

Commissioner for Patents:

This brief is in furtherance of the Notice of Appeal, filed in this case on July 27, 2004. The fees required under Section 1.17(c), and any required request for extension of time for filing this brief and fees therefor, are dealt with in the accompanying transmittal letter.

I. REAL PARTY IN INTEREST

The real party in interest in this appeal is STMicroelectronics S.r.l, which is the assignee of the present application.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences

III. STATUS OF CLAIMS

Claims 1-14, 23-26, and 31-34 are pending and stand rejected. All claims are being appealed.

IV. STATUS OF AMENDMENTS

A Response was filed on June 29, 2004 requesting reconsideration of all of the rejections in the final Office Action dated March 30, 2004. No amendments were requested in the June 29 Response and no other amendments were filed in response to the final Office Action.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The following summary discusses the subject matter of the appealed claims along with references to portions of the specification and drawings that provide support for the claims. The references are provided for exemplary purposes and are not intended to restrict the scope of the claims to the particular embodiments corresponding to the references provided.

Claim 1 is directed to an integrated device that includes first (Th) and second (Te, Me) transistors in emitter switching configuration (see Figures 2-5; page 5, lines 20-24; page 7, lines 1-17). Such an integrated device typically is used as a switch for high-voltage applications, but the invention is not limited to such applications. The device also includes a quenching element (B) that discharges current from the first transistor when the second transistor is turned off. This allows the current on a load driven by the device to be brought to zero.

The quenching element includes a zener diode (Dz1, Dz2) made in polysilicon and formed on a surface of a semiconductor chip (2, 3, 6). The zener diode includes a polysilicon layer 14 having a first zone of first conductivity type and a second zone of second conductivity type that together form at least one PN junction (Figs. 2, 4, 6A-6D; page 6, lines 1-22; page 7, lines 18-25). Positioning the zener diode in the polysilicon layer 14 on the surface of the chip (2, 3, 6) enables the integrated device to occupy a smaller space than prior art devices without compromising the efficiency of the first transistor Th (page 3, lines 20-23).

Claims 9-12 depend on claim 1 and further recite that the quenching element includes two or more zener diodes in back to back connection (Figs. 6B-6D, 8, 10). In claim 9, the anodes of two zener diodes are connected to each other, while in claim 10 the cathodes of the two diodes are connected to each other. In claims 11 and 12, there is a series of couples of zener

diodes with the cathodes of the zener diodes of a couple being connected to each other in claim 11 and with the anodes of the zener diodes of a couple being connected to each other in claim 12.

Independent claim 23 is directed to a device that includes first (Th) and second (Te, Me) transistors formed in a semiconductor substrate (2, 3, 6) (see Figures 2-5; page 5, lines 20-24; page 7, lines 1-17). The device also includes a zener diode (Dz1, Dz2) formed in a polysilicon layer (14) that is formed on an insulating layer (12)on the upper surface of the substrate. The zener diode includes first and second junction regions and is configured to discharge current from a first region of the first transistor when the second transistor is turned off.

Claim 26 depends on claim 23 and further recites that the zener diode is one of a plurality of zener diodes (Dz1, Dz2; Figs. 6B-6D, 8, 10) formed in the polysilicon layer (14). The zener diodes are connected in series and are alternating in plurality. For example, Figure 6B shows a reverse-biased first diode Dz1 and a forward-biased second diode Dz2 while Figure 6C shows a forward-biased first diode Dz1 and a reverse-biased second diode Dz2.

Claim 33 depends on claim 1 and further recites that the emitter region of the first transistor extends as a comb having elongated portions inside the base region. In addition, the polysilicon region includes a plurality of zener diodes distributed along a perimeter of the elongated portions (page 6, lines 23-28). Such an arrangement provides an optimal junction perimeter and may even occupy the same space as an emitter-switching device without an integrated quenching element.

Independent claim 34 includes first (Th) and second transistors (Te, Me) and quenching means for discharging current from the first transistor when the second transistor is turned off (see quenching element B of Figs. 2-5 and 11B; quenching elements B, B' of Fig. 11A, single zener diode of Figs. 2, 4, and 6A; and plural zener diodes of Figs. 6B-6D and 7-10; page 6, lines 1-28; page 7, lines 18-25; page 9, lines 2-17; and page 10, lines 1-7). The quenching means are positioned in a polycrystalline semiconductor layer (14) formed on a second surface of a semiconductor chip (2, 3, 6). The quenching means include a P-N junction formed by first and second zones of first and second conductivities, respectively (See regions labeled P and N of polycrystalline layer 14 in Figs. 2, 4, 6A-6D, 7, and 9).

Claim 42 depends on claim 34 and further recites that the quenching means include first and second zener diodes in back to back connection (See Figs. 6B-6D and 7-10).

Claim 44 depends on claim 34 and further recites that a second conduction region of the first transistor extends as a comb having elongated portions inside the control region. In addition, the polycrystalline semiconductor layer includes a plurality of zener diodes distributed along a perimeter of the elongated portions (page 6, lines 23-28).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claim 38 was rejected under 35 U.S.C. § 112, second paragraph, as being indefinite.

Claims 1-14, 23-26, 31-32, and 34-43 were rejected under 35 U.S.C. 103 as being unpatentable over U.S. Patent No. 6,127,723 to Aiello et al. ("Aiello") in view of U.S. Patent No. 6,207,481 to Yi.

Claims 33 and 34 were rejected under 35 U.S.C. 103 as being unpatentable over Aiello in view Yi and U.S. Patent No. 4,994,880 to Kato et al. ("Kato").

VII. ARGUMENT

A. Indefiniteness Rejection

The Examiner incorrectly indicated that there were not antecedent bases for "the first zone" and "the second zone" in the last four lines of claim 38. Claim 38 depends on claim 34 which recites "a first zone" and "a second zone" in the last three lines of the claim. Thus, claim 38 particularly points out and distinctly claims the invention.

B. Section 103 Rejection Based on Aiello and Yi

1. Introduction

The Federal Circuit has held many times that the Examiner must provide objective evidence of a motivation for combining the teachings of cited references in the manner claimed. *E.g., In re Sang-Su Lee*, 277 F.3d 1338, 1343; 61 USPQ2d 1430, 1433 (Fed. Cir. 2002) (copy enclosed). Further, "this factual question of motivation is material to patentability, and could not be resolved on subjective belief and unknown authority." *Id.* at 277 F.3d 1343-1344;

61 USPQ2d 1433. Moreover, "the mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." *In re Fritch*, 972 F.2d 1260, 1266; 23 USPQ2d 1780, 1783-84.

2. Claims 1-8, 13-14, and 31

The cited prior art does not teach or suggest the invention recited in claims 1-8, 13-14, and 31. In particular, claim 1 recites an integrated device that includes a quenching element having a Zener diode made in polysilicon and formed on a second surface of a semiconductor chip and comprising a polysilicon layer having at least one zone of the first conductivity type and at least one zone of a second conductivity type in order to form at least one P-N junction. Aiello and Yi do not teach or suggest such a quenching element connected as recited in claim 1, for at least three reasons.

First, there is no motivation to combine Aiello with Yi to produce the claimed invention. Aiello shows a diode D1 formed in a monocrystalline epitaxial layer 218 while Yi shows a thin film transistor formed in a polysilicon layer 218 that is separated from a glass substrate 211 by an insulating buffer layer 216. Nothing in Aiello, Yi, or the general knowledge of the prior art provides a reason to replace or combine the monocrystalline diode D1 with the thin film transistor of Yi.

Yi employs a production process typically referred to in the art as silicon-on-insulator (SOI) technology that is not employed together with traditional integrated circuit (IC) technology, like that of Aiello, in which circuit elements are integrated into a single-crystal silicon chip. In SOI devices, like that of Yi, the circuit elements are formed in a polysilicon or amorphous silicon layer that is separated from a glass substrate by an insulating layer. No circuit elements are formed in the substrate. There is nothing in Yi, Aiello, or any general knowledge in the art that would suggest combining an SOI device, like Yi, with a traditional IC device in which circuit elements are incorporated into the substrate.

The Examiner incorrectly asserts that Yi teaches that using polysilicon rather than a single crystal of silicon results in a uniform crystal size and better transistor performance. This assertion is unsupported by any statement in Yi. Rather than comparing polysilicon to

monocrystalline silicon, as in Aiello, Yi simply reports that the method of producing a polysilicon layer in Yi is better than prior art methods of producing polysilicon layers. The Background section of Yi discusses a prior technique of making a polysilicon layer by depositing an amorphous layer of silicon and then crystallizing the amorphous silicon using a heat treatment (col. 1, lines 30-41). Yi then explains that a better polysilicon layer can be made by creating a crystallization seed layer on an amorphous layer of silicon and then crystallizing the amorphous layer by a metal induced lateral crystallization process (col. 3, lines 38-43 and col. 4, lines 1-18). Improving a process of forming a polysilicon layer from an amorphous silicon layer does not provide a motivation changing a zener diode formed in a single crystal of silicon into a zener diode formed in a polysilicon layer positioned above a substrate.

In response to applicants' explanation of the lack of motivation for combining Aiello with Yi, the Examiner responded that "case laws make it clear that choosing an appropriate material is in fact within the level of ordinary skill in the art." This assertion by the Examiner is unsupported and not true. There is no case law stating or implying that choosing an appropriate material is always within the skill of the art. It is clearly true that if the prior art teaches away from employing a particular material, then it would not be within the ordinary skill in the art to use that particular material. For example, it would certainly not be within the ordinary skill in the art to make a transistor integrated in a piece of wood. Moreover, the claimed invention does not merely change materials from a monocrystalline substrate to a polysilicon layer – instead, an entirely new polysilicon layer is added on top of a monocryalline substrate and circuit elements are formed in the polysilicon layer and the monocrystalline substrate.

For the foregoing reasons, the Examiner has not shown any objective evidence of a motivation for combining Yi with Aiello as suggested by the Examiner.

Second, even if one were motivated to combine Yi with Aiello, one still would not create the claimed invention. Claim 1 recites a device that includes a polysilicon quenching on a surface of a semiconductor chip in which first and second transistors are formed. In contrast, Aiello teaches incorporating all of the active elements in a single monocrystalline silicon chip 200 and Yi teaches incorporating a transistor in a polysilicon layer 218 above a glass substrate 211 that does not incorporate any active elements. As such, even if the Examiner were correct that Yi teaches the use of polysilicon rather than monocrystalline silicon, then one would

at best put all of the active elements of Aiello in the polysilicon layer 218 of Yi. Nothing in Aiello or Yi suggest putting one element in polysilicon and the other elements in a monocrystalline silicon substrate. Thus, the Examiner has not provide any objective evidence suggesting the desirability of combining Aiello and Yi in the specific manner suggested by the Examiner to create the claimed invention. *See, In re Fritch, supra.*

Third, even if one were motivated to employ the thin film transistor of Yi on the structure of Aiello, one still would not create the claimed invention. Claim 1 recites that the quenching element, which includes a polysilicon PN junction, is coupled with the base region of the first transistor and with the not drivable terminal of the second transistor. Neither Aiello nor Yi suggest connecting a polysilicon PN junction to a base region or not drivable terminal of integrated transistors. In particular, Yi does not connect the thin film transistor of layer 118 to any regions or terminals of any transistors in the substrate 111. Thus, a hypothetical combination of Yi with Aiello would at most merely position the thin film transistor of Yi in a polysilicon layer above the structure of Aiello, without connecting the thin film transistor as a quenching element between the base terminal of a first transistor and a not drivable terminal of a second transistor.

The Examiner responded simply by noting that the diode D1 of Aiello is connected to the transistors Td1 and Td2, without explaining why one would not simply position the thin film transistor of Yi on the top of the Aiello IC. The Examiner seems to believe that, merely because Yi shows a polysilicon transistor above a glass substrate, one would somehow be motivated to choose to move only the diode D1 of Aiello into a polysilicon layer while still maintaining the same connections. The Examiner also does not explain why the person of ordinary skill would not merely move the transistor Td1 into a polysilicon layer while keeping the diode D1 in the monocrystalline substrate. It appears that the Examiner is improperly using hindsight to pick and choose among the teachings of the prior art based solely on the applicant's disclosure.

For the foregoing reasons, claim 1 is nonobvious in view of the cited prior art. Claims 2-8, 13-14 and 31 depend on claim 1, and thus, are also nonobvious.

3. Claims 9-12

Claims 9-12 are nonobvious in view of the cited prior art for at least two reasons. First, claims 9-12 depend on claim 1, and thus, are nonobvious for the reasons expressed above with respect to claim 1. Second, claims 9-12 recite additional elements that are not taught or suggested by Aiello and Yi.

Aiello and Yi do not teach or suggest a quenching element that includes first and second zener diodes in back to back connection or a series of couple of zener diodes in back to back connection. Instead, Aiello only shows a single zener diode in each embodiment (Dz1 in Figs. 3a, 3b; Dz2 in Fig. 3C; and Dz3 in Figs. 4a, 4b). Aiello never suggest adding another zener diode to any of the embodiments, especially not another zener diode in back to back connection with the first zener diode. Yi does not mention even a single zener diode, and thus, cannot provide the missing teaching.

The Examiner incorrectly points to regions 242/218 and 209/206 of Aiello as showing first and second zener diodes and to regions 239, 242, and 245 as shown plural diodes in back to back connection. The regions 242/218 and 209/206 correspond to the base/collector junctions of transistors Td1 and Th, respectively, and the regions 239, 242, and 245 are part of diode D1, transistor Td1, and transistor Td2, respectively. Nothing in Aiello suggests that the base/collector junctions, diode D1, transistor Td1, or transistor Td2 are zener diodes and they are not inherently zener diodes. A zener diode is "a semiconductor breakdown diode, usually constructed in silicon, in which reverse-voltage breakdown is based on the zener effect," and the zener effect is "nondestructive breakdown in a semiconductor, occurring when the electric field across the barrier region becomes high enough to produce a form of field emission that suddenly increases the number of carriers in this region." McGraw-Hill Dictionary of Scientific and Technical Terms, page 2187, Fifth Edition, McGraw-Hill (1994) (Copy in Evidence Appendix). Nothing in Aiello or the known skill in the art suggests that the base-collector junctions of the transistors Td1, Th, diode D1, transistor Td1, or transistor Td2 exhibit reverse-voltage breakdown based on the zener effect.

Even assuming that the Examiner did not mistakenly identify the regions 242/218, 209/206, 239, 242, and 245 as being zener diodes, those regions still are not in back to back connection between the base terminal of the first transistor and the other not drivable terminal of

the second transistor. The Examiner identifies the region 242 as the base of the first transistor Td1 and either region 206 or 218 as being the other not drivable terminal of the second transistor (see page 2, bottom paragraph)[1]. None of the regions 242/218, 209/206, 239, 242, and 245 are connected in back to back connection between the base 242 of transistor Td1 and either of the regions 206, 218.

For the foregoing reasons, claims 9-12 are nonobvious in view of Aiello and Yi.

4. Claims 23-25 and 32

Although the language of claims 23-25 and 32 differs from that of claim 1, the allowability of claims 23-25 and 32 will be apparent in view of the above discussion of claim 1. In particular, claim 23 recites a zener diode formed in a polysilicon layer formed on an insulating layer on a substrate in which first and second transistors are formed. As discussed above, Aiello and Yi do not teach or suggest a zener diode formed in a polysilicon layer. In addition, by specifically reciting that the polysilicon layer is *on* an insulating layer on the substrate, claim 23 is further distinguished from Aiello, which shows a zener diode Dz1 *in*, rather than *on*, the epitaxial layer 218 and insulating layer 257. Accordingly, claims 23-25 and 32 are nonobvious in view of Aiello and Yi.

5. Claim 26

Claim 26 is nonobvious in view of the cited prior art for at least two reasons. First, claim 26 depends on claim 23, and thus, is nonobvious for the reasons expressed above with respect to claim 23. Second, claim 26 recites additional elements that are not taught or suggested by Aiello and Yi.

Aiello and Yi do not teach or suggest a plurality of zener diodes connected in series, and alternating in polarities. As discussed above with respect to claims 9-12, Aiello only shows a single zener diode in each embodiment (Dz1 in Figs. 3a, 3b; Dz2 in Fig. 3C; and Dz3 in Figs. 4a, 4b). Aiello never suggest adding another zener diode to any of the embodiments,

[1] Even if one were to point to transistor Th as being the first transistor and Td1 as being the second transistor, which corresponds to the way Aiello was discussed in the Background section of the present application, the PN junctions pointed to by the Examiner are still not connected in back to back connection between the base of transistor Th and either the emitter or collection of transistor Td1.

especially not another zener diode connected in series and alternating in polarity with the first zener diode. Yi does not mention even a single zener diode, and thus, cannot provide the missing teachings.

Also similar to the above discussion of claims 9-12, the Examiner incorrectly relies on the regions 242/218, 209/206, 239, 242, and 245 for his assertion that Aiello shows the features recited in claim 26. None of the PN junctions formed by the regions 242/218, 209/206, 239, 242, and 245 are zener diodes connected in series and alternating in polarity.

For the foregoing reasons, claim 26 is nonobvious in view of Aiello and Yi.

6. Claims 34-41 and 43

Although the language of claims 34-41 and 43 differs from that of claim 1, the allowability of claims 34-41 and 43 will be apparent in view of the above discussion of claim 1. In particular, claim 34 recites quenching means including a first P-N junction positioned in a polycrystalline semiconductor layer formed on a surface of semiconductor chip in which first and second transistors are formed. As discussed above with respect to claim 1, Aiello and Yi do not teach or suggest the claimed invention for at least three reasons. First, there is no motivation to combine the thin-film transistor of Yi, which is made according to SOI technology on a glass substrate, with the circuit of Aiello in which the elements are incorporated in a semiconductor substrate using traditional IC technology. Second, even if one did combine Aiello with Yi, one would not obtain the claimed invention because one skilled in the art would not include a circuit portion in the substrate and a circuit portion in the polysilicon layer of Yi. Third, one would not be motivated to connect the thin-film transistor of Yi with the transistors of Aiello in a manner that would discharge current from the first transistor when the second transistor is turned off. Accordingly, claims 34-41 and 43 are nonobvious in view of Aiello and Yi.

7. Claim 42

Claim 42 is nonobvious in view of the cited prior art for at least two reasons. First, claim 42 depends on claim 34, and thus, is nonobvious for the reasons expressed above with respect to claim 34. Second, claim 42 recites additional elements that are not taught or suggested by Aiello and Yi.

Aiello and Yi do not teach or suggest quenching means in which first and second zener diodes in back to back connection. As discussed above with respect to claims 9-12, Aiello only shows a single zener diode in each embodiment. Aiello never suggest adding another zener diode to any of the embodiments, especially not another zener diode in back to back connection with the first zener diode. Yi does not mention even a single zener diode, and thus, cannot provide the missing teachings.

Also similar to the above discussion of claims 9-12, the Examiner incorrectly relies on the regions 242/218, 209/206, 239, 242, and 245 for his assertion that Aiello shows the features recited in claim 42. None of the PN junctions formed by the regions 242/218, 209/206, 239, 242, and 245 are zener diodes in back to back connection.

For the foregoing reasons, claim 42 is nonobvious in view of Aiello and Yi.

C. Section 103 Rejection of Claims 33 and 44 Based on Aiello, Yi, and Kato

1. Claim 33

Claim 33 is nonobvious over the cited prior art for at least two primary reasons. First, Kato does not teach or suggest the elements of claim 1, from which claim 33 depends, that are missing from Aiello and Yi. Second, Aiello, Yi, and Kato do not teach or suggest the additional elements recited in claim 33.

With respect to the elements recited in claim 1, Kato does not teach or suggest a zener diode formed in a polysilicon layer on a semiconductor chip. In fact, Kato does not teach or suggest any zener diode. Moreover, Kato does not provide any motivation for combining Aiello and Yi as suggested by the Examiner. In addition, Kato does not provide a suggestion of how to combine Aiello and Yi as suggested by the Examiner.

With respect to the elements recited in claim 33, Aiello, Yi, and Kato do not teach or suggest that the emitter region of a first transistor extends as a comb having elongated portions inside the base region and the polysilicon region includes plural zener diodes distributed along a perimeter of the elongated portions. Kato discloses a comb-shaped emitter 35, but the Examiner does not point to any teaching in the prior art to include plural zener diodes distributed along a

perimeter of the elongated portions of the emitter region. As discussed above, Yi and Kato do not even mention any zener diodes.

Aiello shows only one zener diode (Dz1, Dz2, Dz3) in each of the embodiments of Figs. 3a, 3c, and 4a and none of those zener diodes is along a perimeter of an emitter region. Even if one were to believe that the PN junctions at regions 242/218, 209/206, 239, 242, and 245 were zener diodes as incorrectly asserted by the Examiner, those PN junction are still not distributed along a perimeter of an emitter. Instead, those PN junctions are all formed at the base-collector junctions of respective transistors shown in Figure 2a of Aiello. Aiello mentions that the emitter 224 of transistor Th may be comb-shaped (col. 4, lines 1-7), but does not show or suggest any zener diodes along a perimeter of the emitter 224.

For the foregoing reasons, claim 33 is nonobvious in view of the cited prior art.

2. Claim 44

Claim 44 is nonobvious over the cited prior art for at least two primary reasons. First, Kato does not teach or suggest the elements of claim 34, from which claim 44 depends, that are missing from Aiello and Yi. Second, Aiello, Yi, and Kato do not teach or suggest the additional elements recited in claim 44.

With respect to the elements recited in claim 34, Kato does not teach or suggest a quenching means including a first P-N junction formed in a polycrystalline semiconductor layer on a semiconductor chip. In fact, Kato does not teach or suggest any PN junction in a polycrystalline semiconductor layer. Moreover, Kato does not provide any motivation for combining, or a suggestion of how to combine, Aiello and Yi as suggested by the Examiner.

With respect to the elements recited in claim 44, Aiello, Yi, and Kato do not teach or suggest that the emitter region of a first transistor extends as a comb having elongated portions inside the base region and the polysilicon region includes plural zener diodes distributed along a perimeter of the elongated portions. As discussed above, both Kato and Aiello mention a comb-shaped emitter region, but none of the references includes any teaching to include plural zener diodes distributed along a perimeter of the elongated portions of the emitter region. For the foregoing reasons, claim 44 is nonobvious in view of the cited prior art.

VIII. CLAIMS APPENDIX

1. (Previously Presented) An Integrated device in emitter switching configuration, said device being integrated in a chip of semiconductor material of a first conductivity type, said chip having a first surface and a second surface opposite to each other, said device comprising:

a first transistor having a base region, an emitter region and a collector region;

a second transistor having a not drivable terminal for collecting charges, which is connected with the emitter terminal of the first transistor; and

a quenching element that discharges current from the first transistor when said second transistor is turned off, said quenching element being coupled with the base region of the first transistor and with the not drivable terminal of the second transistor, said quenching element having at least one Zener diode made in polysilicon, said at least one polysilicon Zener diode being formed on the second surface of said chip and comprising a polysilicon layer having at least one zone of the first conductivity type and at least one zone of a second conductivity type in order to form at least one P-N junction.

2. (Original) The Integrated device according to claim 1, wherein said chip comprises a first region of the second conductivity type which extends from the second surface into the chip and a second region of the first conductivity type which extends from the second surface into the first region, and the first region, the second region and a portion of the chip comprised between the first region and the first surface forming respectively the base region, the emitter region and the collector region of the first transistor.

3. (Original) Integrated device according to claim 2, wherein said first transistor and said second transistor are bipolar transistors and said chip comprises a third region of the second conductivity type which extends from the second surface into the second region and a fourth region of the first conductivity type which extends from the second surface into the

third region, each of the second region, of the third region and of the fourth region forming respectively the collector region, the base region and the emitter region of the second transistor.

4. (Previously Presented) Integrated device according to claim 2, comprising a bipolar third transistor connected with the first transistor in a Darlington configuration wherein the emitter terminal of the first transistor is connected with a base terminal of the third transistor and the collector terminal of the first transistor is connected with a collector terminal of the third transistor.

5. (Original) Integrated device according to claim 2, wherein said second transistor is a MOS transistor and said chip comprises a couple of third regions of the second conductivity type which extend from the second surface into the second region and a couple of fourth regions of the first conductivity type which extend from the second surface into each one of third regions, each of the second region, of the third regions and of the fourth regions forming respectively the drain region, the body region and the source region of the second transistor.

6. (Original) Integrated device according to claim 1, wherein said first conductivity type of the semiconductor material is of N-type and said second conductivity type of semiconductor material is of P-type.

7. (Original) Integrated device according to claim 1, wherein said first conductivity type of the semiconductor material is of P-type and said second conductivity type of semiconductor material is of N-type.

8. (Original) Integrated device according to claim 1, wherein said at least one polysilicon Zener diode comprises a polysilicon Zener diode the cathode of which is connected with the base terminal of the first transistor and the anode of which is connected with said other not drivable terminal of the second transistor and said polysilicon layer comprises only one P-N junction.

9. (Original) Integrated device according to claim 1, wherein said at least one polysilicon Zener diode comprises first and second polysilicon Zener diodes in back to back connection wherein the anode of the first Zener diode is connected with the anode of the second Zener diode and the cathode of the first Zener diode is connected with the base terminal of the first transistor and the cathode of the second Zener diode is connected with said other not drivable terminal of the second transistor and said polysilicon layer comprises two P-N junctions.

10. (Original) Integrated device according to claim 1, wherein said at least one polysilicon Zener diode comprises first and second polysilicon Zener diodes in back to back connection wherein the cathode of the first Zener diode is connected with the cathode of the second Zener diode and the anode of the first Zener diode is connected with the base terminal of the first transistor and the anode of the second Zener diode is connected with said other not drivable terminal of the second transistor and said polysilicon layer comprises two P-N junctions.

11. (Original) Integrated device according to claim 1, wherein said at least one polysilicon Zener diode comprises a series of couples of polysilicon Zener diodes in back to back connection wherein the cathode of the one Zener diode of one couple is connected with the cathode of the other Zener diode of the same couple and so on and the anode of the first Zener diode is connected with the base terminal of the first transistor and the anode of the last Zener diode is connected with said other not drivable terminal of the second transistor and said polysilicon layer comprises a series of P-N junctions.

12. (Original) Integrated device according to claim 1, wherein said at least one polysilicon Zener diode comprises a series of couples of polysilicon Zener diodes in back to back connection wherein the anode of the one Zener diode of one couple is connected with the anode of the other Zener diode of the same couple and so on and the cathode of the first Zener diode is connected with the base terminal of the first transistor and the cathode of the last Zener diode is connected with said other not drivable terminal of the second transistor and said polysilicon layer comprises a series of P-N junctions.

13. (Original) Integrated device according to claim 1, wherein said at least one polysilicon Zener diode is formed on the second surface of the chip in a zone over an insulated layer.

14. (Original) Integrated device according to claim 1, comprising a diode the cathode of which is connected with the collector terminal of the first transistor and the anode of which is connected with said other not drivable terminal of the second transistor, said diode conducing when the voltage value at the collector terminal becomes lower than the voltage value at the other not drivable terminal of the second transistor.

15.-22. (Cancelled)

23. (Original) A device, comprising:

a semiconductor substrate of a first type of conductivity;

a first region having a second type of conductivity formed in the semiconductor substrate;

a second region having the first type of conductivity formed over and in contact with the first region, the first and second regions and a portion of the substrate underlying the first region forming base, emitter and collector, respectively, of a first transistor;

a second transistor formed in the substrate and including a third region having the first type of conductivity, formed over and in contact with the second region;

the second transistor also including a fourth region having the second type of conductivity, formed in the third region;

an insulating layer selectively formed on an upper surface of the substrate;

a polysilicon layer selectively formed on the insulating layer; and

a zener diode formed in the polysilicon layer and including first and second junction regions having first and second types of conductivity, respectively, the diode being configured to discharge current from the first region when the second transistor is turned off.

24. (Original) The device of claim 23 wherein the second transistor is a bipolar transistor and further includes a fifth region having the first type of conductivity and formed in the fourth region, the third, fourth and fifth regions comprising collector, base and emitter, respectively, of the second transistor.

25. (Original) The device of claim 23 wherein the second transistor is a MOS transistor and further includes:

a fifth region having the second type of conductivity, formed in the third region and separated from the fourth region by a portion of the third region;

sixth and seventh regions having the first type of conductivity and formed in the fourth and fifth regions, respectively; and

a polysilicon region formed on the insulating layer, apart from the polysilicon layer and over the portion of the third region, the polysilicon region, the sixth and seventh regions, and the fourth region comprising gate, source and drain, respectively, of the MOS transistor.

26. (Original) The device of claim 23 wherein the zener diode is one of a plurality of zener diodes formed in the polysilicon layer, the plurality of diodes connected in series, and alternating in polarities.

27.-30. (Cancelled)

31. (Previously Presented) The integrated device of claim 1 wherein said quenching element is on a first side of the second surface, and wherein substantially all semiconducting regions are on a second side of the second surface.

32. (Previously Presented) The device of claim 23 further comprising:

the first, second, third, and fourth regions formed on a first side of the insulating layer; and

the polysilicon layer selectively formed on a second side of the insulating layer.

33. (Previously Presented) The integrated device of claim 1 wherein the emitter region of the first transistor extends as a comb having elongated portions inside the base region and the polysilicon region includes a plurality of zener diodes distributed along a perimeter of the elongated portions.

34. (Previously Presented) An integrated device integrated in a chip of semiconductor material of a first conductivity type, the chip having a first surface and a second surface opposite to each other, the device comprising:

a first transistor having a control region and first and second conduction regions;

a second transistor having a control region and first and second conduction regions, the first conduction region of the second transistor being connected to the second conduction region of the first transistor; and

quenching means for discharging current from the first transistor when the second transistor is turned off, the quenching means being connected between the control terminal of the first transistor and the second conduction region of the second transistor, being positioned in a polycrystalline semiconductor layer formed on the second surface of the chip, and including a first zone of the first conductivity type and a second zone of a second conductivity type in order to form a first P-N junction.

35. (Previously Presented) The integrated device of claim 34, wherein the control region of the second transistor includes a first region of the second conductivity type that extends from the second surface into the chip, the second conduction region of the second transistor includes a second region of the first conductivity type the extends from the second surface into the first region, and the first conduction region of the second transistor includes a third region of the first conductivity type positioned between the first region and the first surface.

36. (Previously Presented) The integrated device of claim 35, wherein the first transistor and the second transistor are bipolar transistors, the second conduction region of the first transistor includes the third region, the first conduction terminal of the first transistor includes a portion of the chip between the third region and the first surface, and the control

region of the first transistor includes a fourth region positioned between the third region and the portion of the chip between the third region and the first surface.

37. (Previously Presented) The integrated device of claim 34 wherein the second conduction region of the first transistor includes a first buried region of the first conductivity type, the control region of the first transistor includes a second buried region of the second conductivity type, and the first conduction region includes a portion of the chip between the second buried region and the first surface.

38. (Previously Presented) The integrated device of claim 37 wherein the second conduction region of the second transistor includes a region of the first conductivity type extending from the second surface into the chip, the device further comprising:

a sinker region that extends from the second surface of the chip to the second buried region;

a first conductive connector positioned on the second surface and connecting the sinker region to the first zone; and

a second conductive connector positioned on the second surface and connecting the second conduction region of the second transistor to the second zone.

39. (Previously Presented) The integrated device of claim 34 wherein the first transistor is a bipolar transistor and the second transistor is a field-effect transistor.

40. (Previously Presented) The integrated device of claim 34, further comprising a bipolar third transistor connected with the first transistor in a Darlington configuration wherein an emitter terminal of the first transistor is connected with a base terminal of the third transistor and a collector terminal of the first transistor is connected with a collector terminal of the third transistor.

41. (Previously Presented) The integrated device of claim 40 wherein the quenching means includes first and second zener diodes connected respectively between the

second conduction terminal of the second transistor and base terminals of the first and third transistors.

42. (Previously Presented) The integrated device of claim 34 wherein the quenching means includes first and second zener diodes in back to back connection.

43. (Previously Presented) The integrated device of claim 34, further comprising an insulating layer positioned between the polycrystalline semiconductor layer and the second surface of the chip.

44. (Previously Presented) The integrated device of claim 34 wherein the second conduction region of the first transistor extends as a comb having elongated portions inside the control region of the first transistor and the polycrystalline semiconductor layer includes a plurality of zener diodes distributed along a perimeter of the elongated portions.

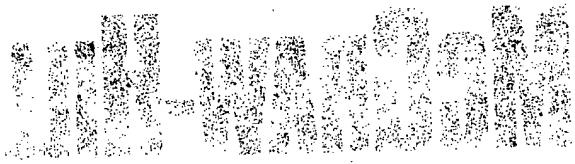
McGraw-Hill Dictionary of Scientific and Technical Terms

Fifth Edition

Sybil P. Parker
Editor in Chief

McGraw-Hill, Inc.
New York San Francisco Washington, D.C.
Auckland Bogotá Caracas Lisbon London Madrid Mexico City Milan
Montreal New Delhi San Juan Singapore Sydney Tokyo Toronto

On the cover: Photomicrograph of crystals of vitamin B_1.
(*Dennis Kunkel, University of Hawaii*)



McGRAW-HILL DICTIONARY OF SCIENTIFIC AND TECHNICAL TERMS, Fifth Edition

4 5 6 7 8 9 0 DOW/DOW 9 9 8

ISBN 0-07-042333-4

Library of Congress Cataloging-in-Publication Data

McGraw-Hill dictionary of scientific and technical terms /
Sybil P. Parker, editor in chief..—5th ed.
p. cm.
ISBN 0-07-042333-4
1. Science—Dictionaries. 2. Technology—Dictionaries.
I. Parker, Sybil P.
Q123.M34 1993
503—dc20 93-34772
CIP

INTERNATIONAL EDITION

When ordering this title, use ISBN 0-07-113584-7.

Z

ZAA spectrometry *See* Zeeman-effect atomic absorption spectrometry. { ˌzē¦āˌā spek'träm·ə·trē }

Zalambdalestidae [PALEON] A family of extinct insectivorous mammals belonging to the group Proteutherea; they occur in the Late Cretaceous of Mongolia. { zəˌlam·dəˈlesˌtəˌdē }

Zanclidae [VERT ZOO] The Moorish idols, a family of Indo-Pacific perciform fishes in the suborder Acanthuroidei. { 'zaŋˌklə,dē }

Zanzibar gum [MATER] A combustible, hard, fossil-type copal, which is insoluble in most solvents and melts at about 245°C; used in varnishes. { 'zanˌzəˌbär ˌgəm }

Zapodidae [VERT ZOO] The Northern Hemisphere jumping mice, a family of the order Rodentia with long legs and large feet adapted for jumping. { zəˈpōidˌəˌdē }

zaratite [MINERAL] $Ni_3(CO_3)(OH)_4{\cdot}4H_2O$ An emerald-green mineral consisting of a hydrous basic nickel carbonate and occurring in incrustations or compact masses. { 'zarˌəˌtīt }

zastruga *See* sastruga. { 'zasˌtrəˌgə }

Z axis [CRYSTAL] The optical axis of a quartz crystal, perpendicular to both the *x* and *y* axes. [MATH] One of the three axes in a three-dimensional cartesian coordinate system; in a rectangular coordinate system it is perpendicular to the *x* and *y* axes. { 'zē ˌak·səs }

Z^0 boson [PARTIC PHYS] An intermediate vector boson which has zero electric charge and mediates the neutral current weak interactions. Also known as Z^0 particle. { 'zē¦zirˌō 'bōˌsän }

Z cam [ASTRON] A representative type of variable star; it is eruptive with a cycle of about 10–600 days; magnitude ranges from 2 to 6. { 'zē ˌkam }

Z Camelopardalis stars [ASTRON] A class of dwarf novae which exhibit unpredictable, and sometimes very protracted, pauses in the decline from maximum to minimum brightness. { 'zē kəˌmel·ə'pärd·əl·əsˌstärz }

Z coefficient [QUANT MECH] A coefficient used in the transformation between modes of coupling eigenfunctions of three angular momenta, and especially in calculating matrix elements for beta decay and similar problems. { 'zē ˌkōˌfiˈshənt }

Z coordinate [MATH] One of the coordinates of a point in a three-dimensional coordinate system, equal to the directed distance of a point from the plane of the *x* and *y* axes, measured along a line parallel to the *z* axis. { 'zē kōˌördˈənˌət }

zebra [VERT ZOO] Any of three species of African mammals belonging to the family Equidae distinguished by a coat of black and white stripes. { 'zēbrə }

zebu [VERT ZOO] A domestic breed of cattle, indigenous to India, belonging to the family Bovidae, distinguished by long drooping ears, a dorsal hump between the shoulders, and a dewlap under the neck; known as the Brahman in the United States. { 'zēˌbü }

Zechstein [GEOL] A European series of geologic time, especially in Germany: Upper Permian (above Rothliegende). { 'zekˌshtīn }

Z-bar [CIV ENG] A metal member, whose cross section has a modified Z shape; the internal angles are slightly less than 90°. { 'zēˌbär }

Zeeman displacement [SPECT] The separation, in wave numbers, of adjacent spectral lines in the normal Zeeman effect for a unit magnetic field, equal (in centimeter-gram-second Gaussian units) to $e/4\pi mc^2$, where e and m are the charge and mass of the electron, or to approximately 4.67×10^{-5} (centimeter)$^{-1}$(gauss)$^{-1}$. { 'zāˌmən diˌsplās·mənt }

Zeeman effect [SPECT] A splitting of spectral lines in the radiation emitted by atoms or molecules in a static magnetic field. { 'zāˌmən iˌfekt }

Zeeman-effect atomic absorption spectrometry [SPECT] A type of atomic absorption spectrometry in which either the light source or the sample is placed in a magnetic field, splitting the spectral lines under observation into polarized components, and a rotating polarizer is placed between the source and the sample, enabling the absorption caused by the element under analysis to be separated from background absorption. Abbreviated ZAA spectrometry. { ¦zē·mən iˌfekt əˌtäm·ikˌəpˌsȯrp·shən spek'träm·ə·trē }

Zeeman energy [ATOM PHYS] The energy of interaction between an atomic or molecular magnetic moment and an applied magnetic field. { 'zāˌmən ˌen·ərˌjē }

Zeiformes [VERT ZOO] The dories, a small order of teleost fishes, distinguished by the absence of an orbitosphenoid bone, a spinous dorsal fin, and a pelvic fin with a spine and five to nine soft rays. { ˌzē·əˈfȯrˌmēz }

zein [MATER] A combustible, white to yellowish protein powder derived from corn; insoluble in water, soluble in dilute alcohol; used in inks, fibers, microencapsulation, and coatings for paper and food. { 'zē·ən }

Zemorrian [GEOL] A North American stage of Oligocene and Miocene geologic time, above Refugian and below Saucesian. { zəˈmȯrˌē·ən }

Zener breakdown [ELECTR] Nondestructive breakdown in a semiconductor, occurring when the electric field across the barrier region becomes high enough to produce a form of field emission that suddenly increases the number of carriers in this region. Also known as Zener effect. { 'zē·nərˈbrākˌdaun }

Zener diode [ELECTR] A semiconductor breakdown diode, usually constructed of silicon, in which reverse-voltage breakdown is based on the Zener effect. { 'zē·nərˈdīˌōd }

Zener diode voltage regulator *See* diode voltage regulator. { 'zē·nərˈdīˌōd 'vōl·tijˌreg·yəˌlād·ər }

Zener effect *See* Zener breakdown.

Zener voltage *See* breakdown voltage. { 'zē·nərˌvōl·tij }

zenith [ASTRON] That point of the celestial sphere vertically overhead. { 'zē·nəth }

zenithal chart *See* azimuthal chart. { 'zē·nə·thəl 'chärt }

zenithal hourly rate [ASTRON] The number of meteors in a meteor shower which would be observed per hour if the radiant of the meteor shower were overhead and there were no moonlight. { 'zē·nə·thəl 'aur·lē 'rāt }

zenithal rain [METEOROL] In the tropics or subtropics, the rainy season which recurs annually or semiannually at about the time that the sun is most nearly overhead (at zenith). { 'zē·nə·thəl 'rān }

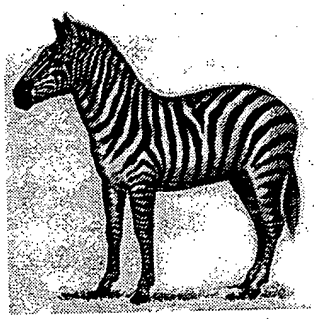
zenith angle [ASTRON] The angle between the direction to the zenith and the direction of a light ray. { 'zē·nəth ˌaŋ·gəl }

zenith distance [ASTRON] Angular distance from the zenith; the arc of a vertical circle between the zenith and a point on the celestial sphere, measured from the zenith through 90°, for bodies above the horizon. Also known as co-altitude. { 'zē·nəth ˌdis·təns }

zenith telescope [OPTICS] A type of telescope that is fixed in the vertical or moves only a small amount from the vertical; it is used to get positional measurement of stars moving near the zenith. { 'zē·nəthˌtel·əˌskōp }

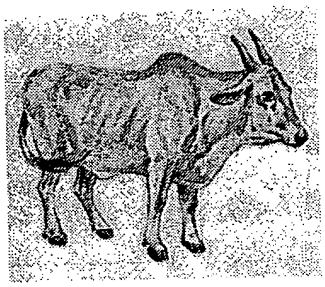
zenocentric coordinates [ASTRON] Coordinates that indi-

ZEBRA



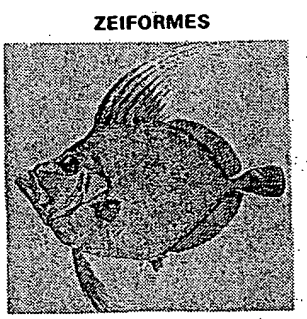
Grevy's zebra *(Equus grevyi)*.

ZEBU



Zebu, or Brahman, a domestic breed of cattle.

ZEIFORMES



John dory *(Zenopsis ocellata)*.

X. RELATED PROCEEDINGS APPENDIX

There are no related proceedings.

Respectfully submitted,
Seed Intellectual Property Law Group PLLC

Robert Iannucci
Registration No. 33,514

RXI:lmt

Enclosures:
Postcard
Check
Transmittal Form
Fee Transmittal Form (+ copy)

701 Fifth Avenue, Suite 6300
Seattle, Washington 98104-7092
Phone: (206) 622-4900
Fax: (206) 682-6031

517417_1.DOC

EXPRESS MAIL NO. **EV529823452US**

FEE TRANSMITTAL for FY 2004

Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27.

TOTAL AMOUNT OF PAYMENT ($) **330.00**

Complete if Known	
Application Number	10/032,289
Filing Date	December 21, 2001
First Named Inventor	Sergio Tommaso Spampinato
Examiner Name	Dana Farahani
Art Unit	2814
Attorney Docket No.	853063.497

METHOD OF PAYMENT

☒ Payment Enclosed:
☒ Check ☐ Credit card ☐ Money Order ☐ Other

☐ Deposit Account:

Deposit Account Number: 19-1090

Deposit Account Name: Seed Intellectual Property Law Group PLLC

The Director is authorized to *(check all that apply)*

☐ Charge fee(s) indicated below ☒ Credit any overpayments
☐ Charge any additional fee(s) during the pendency of this application
☐ Charge fee(s) indicated below, **except for the filing fee**
☒ Charge any deficiencies

to the above-identified deposit account.

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee($)	Small Entity Fee Code	Small Entity Fee($)	Fee Description	Fee Paid
1001	770	2001	385	Utility filing fee	
1002	340	2002	170	Design filing fee	
1003	530	2003	265	Plant filing fee	
1004	770	2004	385	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($) 0

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

			Extra Claims		Fee from below		Fee Paid
Total Claims		-** =		*		=	
Independent Claims		-** =		*		=	
Multiple Dependent						=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	86	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple dependent claim, if not paid
1204	86	2204	43	** *Reissue independent claims over original patent*
1205	18	2205	9	** *Reissue claims in excess of 20 and over original patent*

SUBTOTAL (2) ($) 0

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet.	
1053	130	1053	130	Non-English specification	
1812	2520	1812	2520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1840*	1805	1840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1480	2254	740	Extension for reply within fourth month	
1255	2010	2255	1005	Extension for reply within fifth month	
1401	330	2401	165	Notice of Appeal	
1402	330	2402	165	Filing a brief in support of an appeal	330
1403	290	2403	145	Request for oral hearing	
1451	1510	1451	1510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive – unavoidable	
1453	1330	2453	665	Petition to revive – unintentional	
1501	1330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	2809	385	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	770	2810	385	For each additional invention to be examined (37 CFR § 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	
Other fee (specify) ____					

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 330

SUBMITTED BY

Name (Print/Type)	Robert Iannucci	Registration No. Attorney/Agent	33,514
Signature		Date	September 27, 2004

Customer Number 00500